

Remarks/Arguments

Applicants thank Examiner Anya for the careful examination of this application and the clear explanation of the claim rejections. In response, applicants amended claims 33, 34, 35, 36, 38, 39 and inserted a new claim 40. Detail explanation of the amendments follows:

1. In claim 33, applicants added an element of “an oxide layer overlying the carbide layer.” What distinguishes this element over the references cited in the Office action is the etching selectivity required of this layer – a structure property not disclosed in the references.

This requirement is fully supported in the specification. Please see Fig. 13 and the explanation associated with the embodiment. In the embodiment the selectivity of the oxide layer to the carbide layer is greater than 10:1. This structural property is clearly depicted in Fig. 13, wherein the oxide layer etching practically stops at the carbide layer.

The Schuegraf reference US 6,620,732 (the ‘732 reference) discloses a method for controlling critical dimension in a polycrystalline silicon emitter. As stated in the Office action, it discloses an emitter-base dielectric stack comprising a carbide layer sandwiched between oxide layers.¹ The oxide layer overlying the carbide, however, has a very different property.

As depicted in Fig. 2 of the ‘732 reference, step 276 describes a step that “selective etch anti-reflective coating and amorphous silicon layer without etching underlying etch stop layer.” In Fig. 3A, element 374 depicts the result of the etch step, in which the ARC coating and the amorphous Si layer are etched in one etch step. The detail of the etch step is described in the specification:

Continuing with FIGS. 2 and 3A, step 276 of flowchart 200 comprises selectively etching ARC 346 and amorphous silicon layer 344 of structure 374. The purpose of etching is to open a "window" onto top surface 324 of base 320. The window will allow for subsequent formation of an emitter

¹ Office action, p. 2. § 3, 5/24/2004.

comprised of N-type polycrystalline silicon on top surface 324 of base 320. The etching is done selectively, i.e. etchants are used which etch silicon oxynitride ARC 346 and amorphous silicon layer 344 but do not substantially etch silicon dioxide etch stop layer 342.²

Although this paragraph describes a process step, it is well recognized in the art of fabrication of semiconductor devices that in order to create a structure such as depicted in Fig. A, step 376 of the '732 reference, it is necessary that the property of the ARC layer be so that its etch-rate not be substantially different to the etch-rate of the amorphous silicon layer. Since claim 1 requires an oxide layer that is resistive to a carbide etching process, the oxide layer / carbide layer combination must necessarily distinguish to the structure disclosed in the '732 reference.

The secondary reference relied on in the Office action is the Schuegraf reference US 6,444,535 (the '535 reference). It discloses a method to reduce emitter to base capacitance and related structure. It discloses a structure wherein there is a silicon-germanium base region 220, a dielectric layer 270, and a polycrystalline silicon layer 260 deposited on the dielectric layer.³ It does not disclose an oxide layer overlying a carbide layer.

Because neither reference discloses an element in claim 1 as amended, they do not establish prima facie obviousness. Therefore, claim 1 stands patentable.

2. Claims 34, 35, 36, 38, and 39 are amended to describe the invention more clearly.

3. Claims 34 – 39 depend directly or indirectly on the now patentable claim 33. At least to the extent that they depend on claim 33, the dependent claims 34 – 39 stand patentable.

4. The new claim 40 describes a bipolar transistor. Among the elements of limitation, claim 40 requires a 4-layered emitter-base dielectric stack. The first layer is a thermal oxide layer and the second layer is a deposited layer. The structures of these two layers are different because they are formed differently. For

² US 6,620,732, col. 6, ll. 56-65.

³ See US 6,444,535, col. 5. l. 47 – col. 6, l. 2.

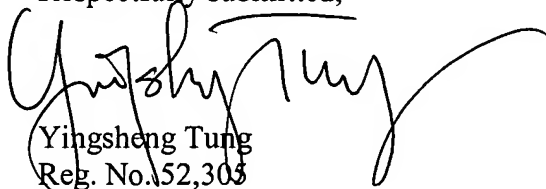
example, the deposited oxide etches at a faster etch-rate in a wet oxide-etch process and the thermal oxide etches at a slower etch-rate. These structures are not disclosed in either references in the Office action.

Another element in claim 40 that is not disclosed in the reference is a second oxide having a favorable dry-etching selectivity with respect to the carbide layer. The element provides for the carbide layer to be the etch-stop for the second oxide and for the second oxide layer to be the hard-mask for the carbide layer.

Because the references relied upon in the Office action do not disclose these elements in claim 40, claim 40 stands patentable.

In summary, applicants respectfully submit that, as amended, the application is in allowable form; pending claims 33 – 40 distinguish over the '535 and '732 references upon which the Office action relied. Applicants respectfully request further examination of this application and timely allowance of the pending claims.

Respectfully submitted,



Yingsheng Tung
Reg. No. 52,303
Attorney for Applicants

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5355
(972) 917-4418 (fax)